Special issue on Energy Efficient Architectures for Embedded Systems

In the last decades, a significant boost in embedded computing systems performance has been observed in several different domains, mostly due to technology scaling and to the ever increasing exploitation of parallel processing architectures.

However, although conventional approaches relying on homogeneous/heterogeneous chip-multiprocessor aggregates already allow achieving a significant performance level, important compromises are necessary in order to cope with the strict energy efficiency requirements present in embedded application domains (e.g. mobile, battery supplied and hand-held devices).

As a consequence, energy efficiency is gradually becoming one fundamental constraint and requisite for embedded systems design, often requiring the adoption of new technologies and micro-architecture design approaches.

This Special Issue (SI) of the EURASIP Journal on Embedded Systems (Springer) entitled ``Energy Efficient Architectures for Embedded Systems'' is mainly focused on new design and development trends of energy efficient processing architectures for embedded systems. The collection of papers presented here emphasizes several aspects of this research domain, including not only architectures and specific design methods, but also more technological aspects related to micro-architecture design, memory hierarchies, communication mechanisms and tools/algorithms for energy/power management and control.

The call for papers resulted in 9 manuscript submissions. For each submission, at least two reviewers examined its quality, together with the guest editors and the editors-in-chief. Finally, 4 papers were selected for publication that cover the following three prominent topics in embedded system design: computer microarchitectures for energy efficiency; energy/power models and management strategies; and energy efficient memory hierarchy subsystems.

%JESY-D-15-00014
The paper entitled ``A hybrid fixed-function and microprocessor solution for high-throughput broad-phase collision detection'', by Muiris Woulfe and Michael Manzke, presents a hybrid processing system spanning a fixed-function microarchitecture and a general-purpose microprocessor, designed to increase the throughput and reduce the power dissipation of collision detection relative to what can be achieved using CPUs or GPUs alone. The primary component is one of two novel microarchitectures designed to perform the principal elements of broad-phase collision detection. Both microarchitectures consist of processing pipelines comprising a plurality of memories, which rearrange the input into a format that maximizes parallelism and bandwidth. The two microarchitectures are combined with the remainder of the system through an original method for sharing data between a ray tracer and the collision-detection microarchitectures to minimize data structure construction costs. According to the presented experimental evaluation using several benchmarks of varying object counts (for over one million objects), the proposed design attains an acceleration of 812x relative to a CPU and an acceleration of 161x relative to a GPU. Furthermore, it is also characterized by being energy efficient which enables the mitigation of silicon power-density challenges, while making the design amenable to both mobile and wearable computing devices.

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The paper entitled ``Dynamic Power Management for Reactive Stream Processing on the SCC Tiled Architecture'', by Nilesh Karavadara, Michael Zolda, Vu Thien Nga Nguyen, Jens Knoop, and Raimund Kirner, presents an execution framework for Reactive Stream Processing Systems (RSPS) that provides a Dynamic Voltage and Frequency Scaling (DVFS) strategy to optimize the power

consumption. The devised DVFS strategy is able to cope with a variable system load, by adjusting the frequency and voltage (in runtime) to the required computational resources, based on the observation of the input and output rates of the RSPS, as well as on the number of workers waiting for new work, to predict overload and underload situations. In contrast to many other approaches, the devised mechanism does not require the ability to control the power setting of individual computational units, making it suitable for tiled many-core processors like the Intel Single-Chip Cloud Computer (SCC). According to the presented experimental validation run on SCC, the proposed DVFS strategy for RSPS can significantly reduce the resulting energy consumption.

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The paper entitled ``Sensing User Context and Habits for Run-Time Energy Optimization'', by Ismat Chaib Draa, Smail Niar,
Jamel Tayeb, Emmanuelle Grislin, and Mikael Desertot, is focused on optimizing the energy consumption in mobile handheld devices, by observing that the number of active sensors and communication tools impact the energy consumption, battery life and system reliability. Firstly, it presents a tool to analyze the user/application interaction and to understand how the different hardware components are used at run time. Then, it makes use of machine learning methods to identify and classify user behaviors and habits information. By using this tool, a software layer has been developed to control and optimize (at run-time) the system component activities that have the highest impact on the energy consumption. The tool also allows predicting future applications usages. With this approach, screen brightness, CPU frequency, Wi-Fi connectivity and playback sound-level can be optimized while meeting the applications and the user requirements. According to the presented experimental evaluation, the proposed solution can lower the energy consumption by up to 30\% vs. the out-of-the-box power governor, while maintaining a negligible system overhead.

%JESY-D-15-00013
The paper entitled ``Energy-Aware Memory Management for Embedded Multidimensional Signal Processing Applications'', by Florin Balasa, Noha Abuaesh, Cristian V. Gingu, Ilie I. Luican, and Hongwei Zhu, presents an Electronic Design Automation (EDA) methodology for the high-level design of hierarchical memory architectures in embedded data-intensive applications, mainly in the area of multidimensional signal processing. Contrasting to previous works, the problems of data assignment to the memory layers, mapping of signals into the physical memories, and banking the on-chip memory are addressed in a consistent way using a single formal model. To accomplish such objective, the devised memory management framework makes use of techniques specific to the integral polyhedra based dependence analysis. When compared to earlier approaches, the added flexibility of this assignment model led to reductions in both the static and dynamic energy consumption in the hierarchical memory subsystem.

To conclude, the guest editors would like to thank all the authors, reviewers, the editorial staff at Springer and the editors-in-chief for their help and support of this special issue. We are confident that the presented set of research papers constitute r relevant steps towards pursuing the challenging task of coping with the strict energy efficiency requirements that are imposed on embedded system application domains.